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EXAMINER

SHECHTMAN, SEAN P

ART UNIT	PAPER NUMBER
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2125

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/964,490

Applicant(s)

MIYAZAKI ET AL.

Examiner

Sean P. Shechtman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,3-13 and 15-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-13 and 15-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2/1/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. Claims 1, 3-13, 15-22 are presented for examination. Claims 1, 3-13, 15-17, and 21 have been amended. Claims 2, 14, and 23-25 have been canceled.

#### ***Drawings***

2. Objection withdrawn due to the amendment.

#### ***Specification***

3. Objection withdrawn due to the amendment.

#### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 4, 5, 16-17, 19-22, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 1, 4, 5, 16-17, 19-22, are rejected as failing to define the invention in the manner required by 35 U.S.C. 112, second paragraph. The claim(s) are narrative in form and replete with indefinite and functional or operational language. The structure which goes to make up the device must be clearly and positively specified. The structure must be organized and correlated in such a manner as to present a complete operative device. The claim(s) must be in one sentence form only. Note the format of the claims in the patent(s) cited.

5. Claim 5 recites the limitation "the threshold value" in the third paragraph(s). Claim 16-17 recites the limitation "the using amount" in line 4. Claim 16-17 recites the limitation "the threshold value". Claim 20 recites the limitation "the stage" in line 3. Claim 22 recites the

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limitation "the same data" in line 5. There is insufficient antecedent basis for these limitation(s) in the claim(s).

6. Referring to claim 1, the phrase "the step of using" is not clear. Specifically, it is not clear if the step uses the second photomask or if the first photomask has, as a blocker against an exposure light, a second photomask which has a metal film.

7. Referring to claims 4, 19-22, it is not clear what is required to be done "upon exposure treatment"- exceeding threshold value, using a photomask, a blocker against exposure light, an organic material containing organic photosensitive resin film, a metal film?

8. Referring to claims 21, it is not clear what is required to be done "prior to a mass production step"- using a photomask as a blocker against an exposure light, an organic material containing an organic photosensitive resin, exposure treatment?

9. Referring to claim 21, it is not clear what is different from each other, - patterns, data?

10. Examiner further invites the applicant's attention to The MPEP 2173.05(a), which clearly states, in part:

"The meaning of every term used in a claim should be apparent from the prior art or from the specification and drawings at the time the application is filed. Applicants need not confine themselves to the terminology used in the prior art, but are required to make clear and precise the terms that are used to define the invention whereby the metes and bounds of the claimed invention can be ascertained."

11. Due to the number of 35 USC § 112 rejections, the examiner has provided a number of examples of the claim deficiencies in the above rejections, however, the list of rejections may not be all inclusive. Applicant should refer to these rejections as examples of deficiencies and should make all the necessary corrections to eliminate the 35 USC § 112 problems and place the claims in proper format.

12. Due to the vagueness and a lack of clear definition of the terminology and phrases used in the specification and claims, the claims have been treated on their merits as best understood by the examiner.

*Claim Rejections - 35 USC § 102*

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

13. Claims 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 4,136,434 to Thibault.

Referring to claims 15-17, Thibault teaches direct writing treatment using an energy beam (Col. 10, lines 15-16).

14. Claims 1, 10, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 3,767,490 to Alberts.

Referring to claim 1, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the step of using a first photomask which has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin (Fig. 1, elements 14 or 16) or a second photomask which has, as a blocker against an exposure light, a metal film (Fig. 1, element 12), the first or second photomask being selected depending on the production amount or fabrication step of the semiconductor integrated circuit device (Col. 4, lines 38-64; Col. 3, lines 63-65). The examiner asserts that both layers are clearly blockers to exposed light. The examiner asserts that exposing and developing in a conventional manner and according to conventional procedures meets the limitation fabrication step of the

semiconductor integrated circuit or selecting the photomask depending on the... fabrication step of the semiconductor integrated circuit.

Referring to claim 10, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the step of using a first photomask which has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin upon exposure treatment in a step of forming patterns relating to the constitution of a logic circuit (Fig. 1, elements 14 or 16), while using a second photomask which has, as a blocker against an exposure light, a metal film upon exposure treatment in a step of forming patterns relating to a unit cell (Fig. 1, element 12).

Referring to claim 18, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the steps of: (a) forming a first photomask having, as a blocker against an exposure light, an organic material containing an organic photosensitive resin on a semiconductor-integrated-circuit-device evaluator's side (Figs. 1-2, elements 16 or 14); (b) transferring a predetermined pattern onto a semiconductor wafer by exposure treatment with the first photomask, on a semiconductor-integrated-circuit-device maker's side (Figs. 1-2); and (c) evaluating the semiconductor wafer to which the predetermined pattern has been transferred, on the semiconductor-integrated-circuit-device evaluator's side (Col. 5, line 47 – Col. 6, line 15). The claims do not require that the evaluator be different from the maker nor do the claims require the evaluator be located separately from the maker. In an example, Alberts teaches evaluating contact holes (Col. 5, line 47 – Col. 6, line 15).

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15. Claims 1, 3-7, 10, 12, 18, are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 5,776,836 to Sandhu.

Referring to claim 1, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the step of using a first photomask which has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin (Col. 5, lines 56-59) or a second photomask which has, as a blocker against an exposure light, a metal film (Col. 5, lines 62-67), selecting the first or second photomask depending on the production amount or fabrication step of the semiconductor integrated circuit device (Col. 4, line 50 – Col. 5, line 14).

Referring to claims 3 and 5, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) judging whether the production amount of the semiconductor integration circuit device exceeds a predetermined threshold production amount or not; (b) when the production amount of the semiconductor integrated circuit device exceeds the threshold value, judging whether the function of the semiconductor integrated circuit device has been determined or not; (c) when the function has not been determined, using a photomask which has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin film upon exposure treatment (Col. 7, lines 15-48).

Referring to claim 4, Sandhu teaches a fabrication method of a semiconductor integrated circuit device according to claim 3, further comprising the step of using a photomask which has, as a blocker against an exposure light, a metal film upon exposure treatment when the production amount of the semiconductor integrated circuit device is expanded to exceed the threshold value (Col. 5, lines 62-67).

Referring to claims 6, 7, 10, and 12, Sandhu teaches a fabrication method of a semiconductor integrated circuit device according to claim 5, further comprising the step of using a photomask which has, as a blocker against an exposure light, a metal film upon exposure treatment in a stage when the function of the semiconductor integrated circuit device is determined (Col. 5, lines 62-67).

Referring to claim 18, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) forming a first photomask having, as a blocker against an exposure light, an organic material containing an organic photosensitive resin on a semiconductor-integrated-circuit-device evaluator's side (Col. 5, lines 56-59); (b) transferring a predetermined pattern onto a semiconductor wafer by exposure treatment with the first photomask, on a semiconductor-integrated-circuit-device maker's side; and (c) evaluating the semiconductor wafer to which the predetermined pattern has been transferred, on the semiconductor-integrated-circuit-device evaluator's side (Col. 7, lines 15-48).

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 3,767,490 to Alberts in view of U.S. Pat. No. 4,000,054 to Marcantonio.

Referring to claim 8, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the step of using a photomask (Col. 3, lines 39-66), as a blocker against an exposure light (Col. 3, lines 63-65), an organic material containing an organic photosensitive resin upon exposure treatment (Fig. 1, element 14; Col. 8, claim 6;

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Col. 3, lines 1-6) prior to subsequent conventional procedures (Col. 3, lines 64-65) or prior to subsequent deposition or annealing (Col. 5, lines 39-41).

The examiner submits that the claims, as such, do not require that the method not be performed as a mass production step, as clearly set forth in claim 11. That is, the method could be interpreted as being performed as a mass production step prior to another mass production step (see the last paragraph of claim 11). The examiner respectfully submits that the claims, as such, do not even require that the mass production step be made on the semiconductor integrated circuit.

While Alberts teaches the method above, and Alberts teaches the method above prior to subsequent conventional procedures (Col. 3, lines 64-65) or prior to subsequent deposition or annealing (Col. 5, lines 39-41), Albert fails to teach that such subsequent conventional procedures or subsequent deposition or annealing are “a mass production step”.

However, Marcantonio teaches analogous art, wherein a depositing step is performed by batch processing or other mass-production techniques (Col. 7, lines 14-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Alberts with the teachings of Marcantonio to perform deposition in “a mass production step”. One of ordinary skill in the art would have been motivated to combine these references because Marcantonio teaches mass production deposition with high reliability and at low cost (Col. 7, lines 6-14).

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17. Claims 8, 9, 11, 13, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,776,836 to Sandhu as applied to claims 1, 3-7, 10, 12, 18, 23, and 24 above, and further in view of U.S. Pat. No. 4,000,054 to Marcantonio.

Referring to claims 8, 9, 11, 13, and 19-22, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) using a first photomask having, as a blocker against an exposure light, an organic material containing an organic photosensitive resin upon exposure treatment for forming patterns relating to the constitution of a logic circuit of the semiconductor integrated circuit device, (b) using a second photomask having a metal as a blocker against an exposure light upon exposure treatment for forming patterns relating the constitution of the logic circuit in the mass production step of the semiconductor integrated circuit device, and (c) using the second photomask having a metal as a blocker against an exposure light upon exposure treatment for forming patterns relating to a unit cell prior to the mass production step (Col. 4, line 50 – Col. 5, line 14).

Referring to claims 8, 9, 11, 13, and 19-22, Sandhu teaches all of the limitations set forth above, but fails performing a step or steps before or in a mass production step.

However, Marcantonio teaches analogous art, wherein steps are performed before or by batch processing or other mass-production techniques (Col. 7, lines 14-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Sandhu with the teachings of Marcantonio to perform before or by “a mass production step”. One of ordinary skill in the art would have been motivated to combine these references because Marcantonio teaches mass production deposition with high reliability and at low cost (Col. 7, lines 6-14).

18. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,776,836 to Sandhu as applied to claims 1, 3-7, 10, 12, 18, 23, and 24 above, and further in view of U.S. Pat. No. 6,211,013 to Park.

Referring to claim 15, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising, upon forming patterns of the semiconductor integrated circuit device, properly using (a) exposure treatment using a first photomask having, as a blocker against an exposure light, an organic material containing an organic photosensitive resin; (b) another exposure treatment using a second photomask having a metal film as a blocker against an exposure light. Referring to claim 16, Sandhu teaches a fabrication method of a semiconductor integrated circuit device according to claim 15, comprising the steps of: judging whether the using amount of the photomask exceeds a predetermined threshold using amount or not; judging whether the first photomask is usable or not when the using amount of the photomask is less than the threshold value, and carrying out exposure treatment with the first photomask when the first photomask is usable. Referring to claim 17, Sandhu teaches a fabrication method of a semiconductor integrated circuit device according to claim 15, comprising the steps of: judging whether the using amount of the photomask exceeds a predetermined threshold using amount or not; judging whether the second photomask is usable or not when the using amount of the photomask exceeds the threshold value, carrying out exposure treatment with the second photomask when the second photomask is usable, judging whether the first photomask is usable or not when the second photomask is unusable, carrying out exposure treatment with the first photomask when the first photomask is usable (Col. 4, line 50 – Col. 5, line 14).

Referring to claims 15-17, Sandhu teaches all of the limitations set forth above, but fails teach direct writing using e-beam.

However, Park teaches analogous art, including direct writing treatment using an energy beam (Col. 6, claim 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Sandhu with the teachings of Park. One of ordinary skill in the art would have been motivated to combine these references because Park teaches advantageously using e-beam lithography to obtain smaller line width gap, thereby reducing a size of an electrically formed quantum dot down to a few tens of nanometers (Col. 3, lines 37-52).

#### *Response to Arguments*

19. Applicant's arguments filed January 21<sup>st</sup> 2005 have been fully considered but they are not persuasive.

Applicant argues that paragraph 0110 of the instant specification defines the term "photomask" as "having light blocking patterns or light phase shifting patterns formed on a mask substrate. It includes a reticle which contains patterns of several times greater than the final size".

For convenience sake, the examiner has presented this portion of the instant specification below, as well as other portions of the instant specification the examiner believes to be appropriate regarding this argument.

"[0110] 1. Mask (photomask): having light blocking patterns or light phase shifting patterns formed on a mask substrate. It includes a reticle which contains patterns of several times greater than the final size. The "first main surface of a mask" means a surface on which the light

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blocking patterns or light phase shifting patterns have been formed, while the "second surface of the mask" means a surface opposite to the first main surface.

[0111] 2. Conventional mask (second photomask): means an ordinarily employed mask having, on a mask substrate, mask patterns composed of light blocking patterns made of a metal and light transmitting patterns. In this embodiment, it includes a phase shift mask having a means for causing a phase difference in an exposure light transmitting through the mask. A groove made in a mask substrate to a predetermined depth or a transparent or semi-transparent film of a predetermined thickness disposed on a mask substrate serves as a phase shifter for causing a phase difference in an exposure light.

[0112] 3. Resist mask (first photomask): means a mask having a light blocker (light blocking film, light blocking pattern, light blocking region) made of an organic material containing an organic photosensitive resin on a mask substrate. The term "organic material" as used herein embraces a single film of an organic photosensitive resin, an organic photosensitive resin film having, added thereto, a light absorbing material or light attenuating material and a laminate of an organic photosensitive resin film and another film (for example, an antireflection film, light absorbing resin film or light attenuating resin film)."

"[0146] A description will next be made of the mask M. The mask M used in this embodiment is a reticle for transferring original integrated circuit patterns of about 1 to 10 times greater than the final size to a wafer through a reduction projection optics. Here, a mask to be used for the transfer of line patterns to a wafer is exemplified. The technical concept of the present invention is not limited to the mask but can be applied to various ones. It is also applicable to a mask for transferring the above-described hole patterns. *A conventional mask and resist mask which will hereinafter be described are only examples shown to facilitate understanding of the description and a conventional mask and resist mask usable in the present invention are not limited by them.*"

"[0154] In an integrated circuit pattern region of the mask MN4b of FIG. 9, a two-dimensional square light transmitting region 4e having a relatively small area has been formed. This light transmitting region 4e is formed in a region corresponding to the portion of the integrated circuit pattern region of the mask MN4a covered with the light blocking pattern 5b. Light blocking patterns 5a are disposed in this light transmitting region 4e. A more than half of the light transmitting region 4e is surrounded with the light blocking pattern 5b made of a metal. This mask MN4b serves as a mask for transferring patterns of a circuit constituted of a pattern group to be corrected or changed in the semiconductor integrated circuit device. Described specifically, when the pattern must be corrected or changed, only the mask MN4b is replaced with a new one, leading to saving of a manufacturing time. In addition, a material cost, step cost and fuel cost upon mask manufacture can be reduced. Upon exposure treatment, the wafer is subjected to exposure treatment using the masks MN4a and MN4b. After completion of the exposure treatment with these masks MN4a and MN4b, *a resist mask on the wafer is subjected to development or the like, whereby resist patterns are formed on the wafer.*"

The examiner respectfully submits that the definitions provided in paragraphs 110-112 do not provide for an explicit definition of the term photomask. Furthermore, the examiner respectfully notes paragraph 146 of the instant specification that teaches "A conventional mask and resist mask which will hereinafter be described are only examples shown to facilitate understanding of the description and a conventional mask and resist mask usable in the present invention are not limited by them".

Finally, the examiner believes that the instant specification can be interpreted to teach a photomask/resist mask/mask in a variety of ways. While paragraphs 110-112 may describe a photomask/resist mask/mask as "having light blocking patterns or light phase shifting patterns formed on a mask substrate" that "includes a reticle which contains patterns of several times greater than the final size". Paragraph 154 of the instant specification clearly teaches "*a resist mask on the wafer is subjected to development or the like, whereby resist patterns are formed on the wafer*". In photolithography a mask substrate or reticle is above the wafer, not on the wafer as required by the description of the term photomask/resist mask/mask in paragraph 154 of the instant specification. Rather the terminology used in this description (i.e., paragraph 154) of a photomask/resist mask/mask is consistent with the terminology of Alberts and Sandhu. As asserted by both the examiner and applicant (See arguments presented January 21<sup>th</sup> 2005), both Alberts and Sandhu teach a photoresist used as the masking layer.

Hence, the examiner respectfully believes that the term photomask/resist mask/mask was clearly open to multiple views of interpretation, and thus, the examiners interpretation set forth in the previous office action was appropriate.

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Examiner further invites the applicant's attention to The MPEP 2106, which clearly states, in part:

"Office personnel must rely on the applicant's disclosure to properly determine the meaning of terms used in the claims. *Markman v. Westview Instruments*, 52 F.3d 967, 980, 34 USPQ2d 1321, 1330 (Fed. Cir.) (en banc), aff'd, U.S. , 116 S. Ct. 1384 (1996). An applicant is entitled to be his or her own lexicographer, and in many instances will provide an explicit definition for certain terms used in the claims. Where an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as it is used in the claim. *Toro Co. v. White Consolidated Industries Inc.*, 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999) (meaning of words used in a claim is not construed in a "lexicographic vacuum, but in the context of the specification and drawings."). Office personnel should determine if the original disclosure provides a definition consistent with any assertions made by applicant. See, e.g., *In re Paulsen*, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (inventor may define specific terms used to describe invention, but must do so "with reasonable clarity, deliberateness, and precision" and, if done, must "set out his uncommon definition in some manner within the patent disclosure" so as to give one of ordinary skill in the art notice of the change" in meaning) (quoting *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1387-88, 21 USPQ2d 1383, 1386 (Fed. Cir. 1992)). Any special meaning assigned to a term "must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention." *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1477, 45 USPQ2d 1429, 1432 (Fed. Cir. 1998)."

Examiner respectfully submits that instant specification fails to provide "a definition consistent with any assertions made by applicant" (MPEP 2106). Examiner respectfully encourages applicant to amend the claim to better reflect what applicant intends to claim as the invention, and it is for this reason that claimed limitations are believed to be met by the applied prior art and the previous rejection is maintained.

### ***Conclusion***

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. The prior art or art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents or publications are cited to further show the state of the art with respect to an energy beam.

U.S. Pat. No. 4,351,892 to Davis.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean P. Shechtman whose telephone number is (571) 272-3754. The examiner can normally be reached on 9:30am-6:00pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

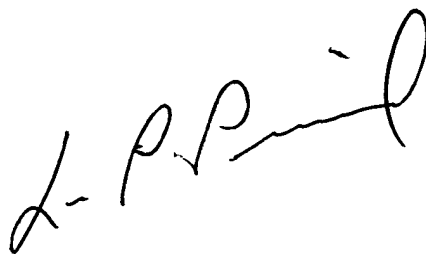
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applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SPS

Sean P. Shechtman

August 4, 2005

A handwritten signature in black ink, appearing to read "L. P. Picard", written diagonally across the page.

**LEO PICARD  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100**